REMARKS

The application includes claims 1-3 and 5-17 prior to entering this amendment.

The examiner rejects claims 1, 3, and 5-17 under 35 U.S.C. § 103(a) as being unpatentable over Cappels, Sr. (U.S. Patent No. 5,731,843) in view of Levantovsky et al. (U.S. Patent No. 6,522,365) and Ichiraku (U.S. Patent No. 6,097,379).

The examiner rejects claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Cappels, in view of Levantovsky, Ichiraku, and Koike et al. (U.S. Patent No. 6,538,648).

The applicant does not amend any claim.

The application remains with claims 1-3 and 5-17 after entering this amendment.

The applicant adds no new matter and requests reconsideration.

Claim Rejections Under § 103

The examiner rejects claims 1, 3, and 5-17 as being obvious over Cappels in view of Levantovsky and Ichiraku. The applicant traverses the rejection for the following reason.

Claim 1 recites that *the phase adjust circuit simultaneously generates a plurality of delayed clock signals by delaying the phase locked loop clock.* The examiner acknowledges that Cappels, Sr. does not disclose the recited limitation, but alleges that Levantovsky teaches the limitation.

Levantovsky discloses in figure 2 "a pixel clock 50 used in sampling the active video portion 36 of an analog signal 10 … shown in various phase relationships with the active video signal 10."[1] Levantovsky's figure 2 discloses various cases (A, B, and C), where the pixel clock 50 has different phase relationship with the active video signal 10. Levantovsky also discloses a method "in which the phase of the pixel clock relative to the active video portion of the horizontal scan lines is adjusted. Changes in the pixel clock phase can affect the image geometry …"[2] Levantovsky also discloses, in figure 8, a phase adjuster module 244 that "generates a phase-adjusted pixel clock at its output 258 in response to the phase control signal and the pixel clock."[3]

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[1] Levantovsky, column 4, lines 48-52.
[2] Levantovsky, step 128 of figure 3 and column 5, lines 39-42. Also see column 6, lines 36-54.
[3] Levantovsky, column 7, lines 43-45.

Put differently, Levantovsky teaches adjusting the phase of a pixel clock signal in response to a phase control signal. Levantovsky, however, does not teach simultaneously generating all three phase adjusted pixel clocks (i.e., Cases A, B, and C) of figure 2, as would be required by claim 1. On the contrary, Levantovsky merely teaches adjusting the phase of a single pixel clock signal. Cases A, B, and C of figure 2 are just three of the various possible ways the pixel clock phase may be adjusted. Levantovsky, then, fails to disclose simultaneously generate a plurality of delayed clock signals by delaying the phase locked loop clock, as would be required by claim 1.

Additionally, the examiner alleges that Cappels' phase adjuster 50 discloscs the recitcd phase adjust circuit and comparator 46 and microprocessor 48 disclose the recited phase detector circuit. Cappels phase adjuster 50 generates an adjusted pixel sampling clock signal 64, which is fed to the comparator 46. The comparator 46 is configured to input only one adjustcd pixel sampling clock signal 64. That is, even if, *arguendo,* the phase adjuster 50 simultaneously generates a plurality of delayed clock signals, the comparator 46 is not structured to accept such a plurality of delayed clock signals. And hence, such a plurality of delayed clock signals generated simultaneously by the phase adjuster 50 would be redundant. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *MPEP 2143.01 III.* The examiner has not provided any motivation, reason, or desirability to incorporate a plurality of simultaneously generated delayed clock signal in Cappels' system. And hence, even if, *arguendo*, Levantovsky teaches (it does not) simultaneously generating a plurality of delayed clock signals by delaying the phase locked loop clock, the examiner has not provided any motivation to apply Levantovsky to Cappels to incorporate such a plurality of signals in Cappels' system.

For at least these reasons, claim 1 is in condition for allowance, along with associated dependent claims 2-3 and 5-17.

Conclusion

The applicant requests reconsideration and expeditious issuance of all remaining claims. The applicant encourages the examiner to call the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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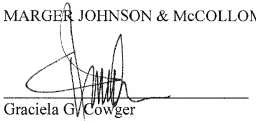

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